IEEE MADRAS SECTION
IEEE COMMUNICATIONS SOCIETY, MADRAS CHAPTER
IEEE COMPUTER SOCIETY, MADRAS CHAPTER
COMPUTER SOCIETY OF INDIA, CHENNAI CHAPTER

cordially invite you for a technical talk by

Mr. S. Sivanantham

Asst. Prof. (Selection Grade) - VLSI Division
School of Electronics Engineering
VIT University, Vellore - 632 014

on the topic

"VLSI for Communication Engineering"

on Saturday, 24th Jul 2010 at 6.00 p.m.

at ISTE Professional Centre, Gandhi Mandapam Road, Chennai – 600 025
(Between AMM School / Kotturpuram Signal & Anna Gem School)

Dr. T. Thyagarajan
Chairman, IEEE Madras Section

Dr. N.R. Alamelu
Chairperson, IEEE COMSOC Madras Chapter

Mr. H.R. Mohan
Chairman, IEEE CS Madras Chapter

Dr. P. Sakthivel
Chairman, CSI Chennai Chapter

Programme

5.30 p.m.: Fellowship & Tea :: 6.00 p.m.: Technical Talk :: 7.30 p.m. : Dinner (Packed)

IEEE MADRAS SECTION
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Abstract of the Talk: VLSI technology is changing very fast towards and rapid developments are taking place. The concept of next generation network is also to integrate the different types of communication technologies and signal processing through VLSI. With the increasing demand it is very essential to get the know how of the VLSI technology for signal processing and communication systems with ensured quality of service. Digital signal processing (DSP) applications are becoming more prevalent in everyday use. Because of this widespread usage and advances in computer technology, the DSP algorithms themselves are being subjected to more demanding specifications. There is a constant need for designing VLSI based systems with lower power, higher speed, and lower area. There is a need for developing new algorithms, architectures, techniques, and design tools. This technical-talk focuses on VLSI CAD tools for communication system design. The tools allow for rapid algorithm development using a functional model library and scripting procedures that automate iterative optimization of algorithm parameters. Implementation tools are linked into the algorithm design environment to allow efficiency in generating hardware designs from algorithm descriptions.